
Nidhi SM

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Bengaluru -560040, Karnataka

SUMMARY

Innovative Electrical Engineer with a proven track record of evaluating electrical systems and applying knowledge of electricity and materials in a beneficial way. Adept in carefully diagnosing and assessing issues, and offering real viable solutions. Skilled in design, prototyping, and testing. Committed to working as a collaborative and positive team member, striving to utilize my knowledge and expertise for optimal engineering results.

CAREER OBJECTIVE

To secure a challenging position in a reputable organization to expand my learnings, knowledge and skills.

SKILLS

Fast Learner
Computer Skills
Interpersonal Skills
Leadership and Teamwork
Effective Time Management
Microsoft Excel
Ability to Work Under Pressure
Leadership Skills
Communication Skills
Microsoft Office
Ability to Work in a Team
Analytical Skills
Decision-making capabilities
Analytical mindset

EDUCATION

Advanced Diploma in ASIC Design - RTL Verification	2024
RV-VLSI Design Center	
Bachelor Degree in Electronics and Communication	2023
Presidency University , with 6.14 CGPA	
PUC	2019
National institute of open schooling , with 69 %	
SSLC	2017
Holy Angels High school , with 66.56 %	

DOMAIN SPECIFIC PROJECT

RV SKILLS CENTRE

Graduate Trainee Engineer

Design and verification of RAM using verilog Description

Created synthesizable able RTL code for RAM using Verilog, complemented by a self-checking test bench to validate Design Under Test (DUT) functionality.

Roles and Responsibilities

- Constrained randomization limitations in Verilog for stimuli generation.
- Difficulty synchronizing multiple initial block statements in the event queue.
- Verilog's inability to declare array data types, hindering test bench development.
- Lack of object-oriented programming concepts in Verilog, impacting reusability of test benches.

RV SKILLS CENTRE

Graduate Trainee Engineer

Verification of FIFO using system verilog Description

Designed FIFO module in Verilog with synthesizable RTL code. Developed versatile verification environment with essential testbench components for rigorous testing across scenarios.

Roles and Responsibilities

- Time-intensive nature of building the testbench using SystemVerilog.
- Synchronizing various data type classes described using object-oriented programming (OOP) concepts. Handling reset and configuration across different components.
- Overcoming complexities in synchronization techniques and creative problem-solving.
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B.TECH ACADEMIC PROJECT

Presidency University

AGRIBOT

Description

"I created an advanced agri-monitoring system during my B.Tech, tailored for large land areas. It tracks soil quality, crop growth, and enables wireless data exchange for enhanced productivity."

Tools

Hardware requirements: 1.ESP32 2.DC Motor 3.Reyal 4.Driver circuit 5.water pump 6.Power source 7.DHT11 Software requirements: Embedded c Arduino ide

Challenges

- Integration of sensors and microcontrollers Achieving seamless wireless communication Rigorous testing and observation for validation Addressing field activity and irrigation challenges